

# LIGHTWAVE COMMUNICATION ICs BEYOND 10 Gb/s

## - DESIGN AND MEASUREMENT CHALLENGES

(Invited Paper)

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### ABSTRACT

Recently emerging lightwave communications technologies have resulted from the remarkable progress in electronic and photonic device technologies as well as in fiber-optic technology and coherent-transmission technology. This paper discusses the state-of-the-art design and measurement technologies for high-speed lightwave communication ICs.

### I. LIGHTWAVE COMMUNICATION ICs

Figure 1 summarizes the optical-fiber transmission technologies. 10-Gb/s transmission systems using the intensity modulation and direct detection (IMDD) method [1] have already been developed, and the transmission bit rate in these systems is limited by the speed of front-end electronic ICs such as the baseband amplifier and decision

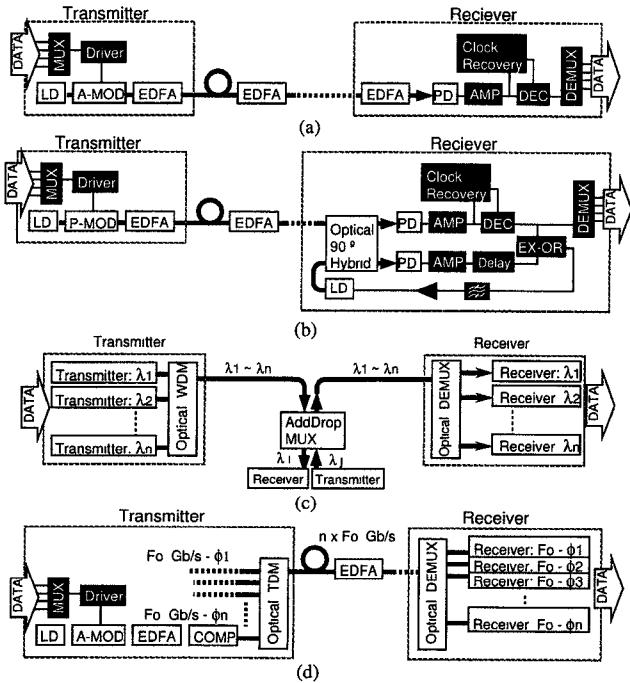


Fig. 1. Typical optical-fiber transmission systems: (a) IMDD system, (b) coherent PSK homodyne system, (c) optical WDM system, and (d) soliton transmission system. MUX multiplexer, LD laser diode, EDFA Er-doped fiber amplifier, PD photo detector, A-MOD amplitude modulator, P-MOD phase modulator, DEC decision IC, EX-OR exclusive-OR, DEMUX demultiplexer, COMP soliton pulse compressor.

ICs. Wavelength division multiplexing (WDM) is a promising way to extend this limit, and 160-Gb/s (20-Gb/s IMDD x 8 channels) transmission has been demonstrated [2].

Coherent transmission requires less optical spectral width than is required for IMDD, thus giving rise to a higher density of wavelength division multiplexing [3]. On the other hand, ultrashort soliton pulses enable noise-free transmission over an infinite distance and have achieved the record bit rate of 160 Gb/s/channel [4]. In these systems, photonic functional elements such as a 90-degree hybrid planer lightwave circuit (PLC), an all-optical multi/demultiplexer, and an add-drop multiplexer PLC are key elements for optical microwave interfaces.

As shown in Fig. 1, the functionality required for the front-end electronic transmitter/receiver ICs is basically the same (multiplexing, amplifying, retiming, regenerating and demultiplexing) for all the transmission systems. Although the WDM and soliton-transmission technology can reduce the transmission bit rate needed for electronic front-end circuits in a single channel, the speed of electronic ICs must be increased beyond 10 Gb/s as the demand on transmission capacity increases to Tb/s.

### II. PROCESS TECHNOLOGY

Semiconductor device technologies applicable to over 10-Gb/s operation are summarized in Table 1. Si bipolar transistors are the most mature and are applicable to the low-speed regime around 10 Gb/s. Si-Ge HBTs and GaAs MESFETs are suited to the medium speed regime (10~30 Gb/s). InAlAs/InGaAs HEMTs and AlGaAs/GaAs HBTs cover the high-end regime beyond 30 Gb/s. Table 2 lists obtainable performances of amplifier and decision ICs at commercial and research/development levels.

Table 1. Record performances for high-speed semiconductor process technologies.

Transistor type	Substrate	Active layer / Minimum size	fT / fmax	Company
Si Bipolar	Si	n-Si, p-Si / 0.8 $\mu$ m	45 GHz / 46 GHz	NEC
HBT	Si	Si-Ge / 1.0 $\mu$ m	85 GHz / 65 GHz	Daimler Benz
MESFET	GaAs	n-GaAs / 0.1 $\mu$ m	113 GHz / 132 GHz	NTT
HEMT	InP	InAlAs/InGaAs / 50 nm	340 GHz / 250 GHz	Hughes
HBT	InP	InP/InGaAs / 2 $\mu$ m	160 GHz / 162 GHz	NTT

Table 2. High-end performances of wideband amplifier and static D-FF ICs at commercial and R&D levels.

Circuit	Items	Commercial level	R&D level
Wideband amplifier IC	Process	0.2- $\mu$ m GaAs MESFET	0.1- $\mu$ m InAlAs/InGaAs HEMT
	3-dB BW	DC to 10 GHz typ.	DC to 50 GHz typ.
	Gain	17 dB typ.	16 dB typ.
	Noise figure	4.7 dB typ.	5 dB typ.
	Power	780 mW max.	1100 mW max.
	Company	NEL	NTT
Static D-FF IC	Process	0.2- $\mu$ m GaAs MESFET	1.5- $\mu$ m AlGaAs/GaAs HBT
	f max	13 Gb/s typ.	40 Gb/s typ. (on wafer)
	Sensitivity	150 mVpp typ.	Not specified
	Power	1.4 W typ.	2.3 W typ. *
	Company	NEL	TOSHIBA

\* This value includes the dissipation of the internal 1:2 selector circuit.

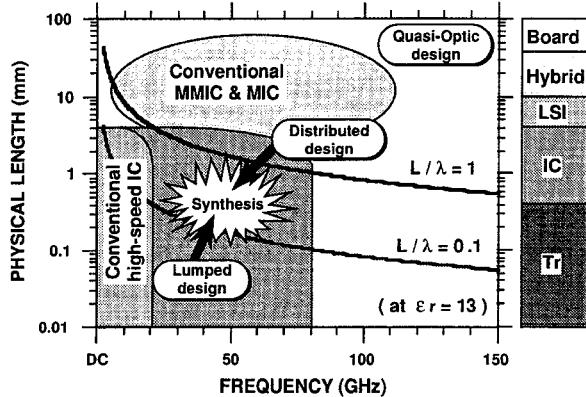


Fig. 2. Physical length ( $L$ ) vs. wavelength ( $\lambda$ ). (GaAs material is assumed, which gives a relative permittivity  $\epsilon_r$  of 13. )

### III. CHALLENGE IN ULTRABROAD-BAND IC DESIGN

As electrical signal frequencies increase beyond 10 GHz, wavelength of the signal approaches to the physical size of IC chips (Fig. 2). This causes substantial difficulties in designing ICs: 1) numerous parasitics, 2) cavity resonance, and 3) bandwidth limitation due to lumped-circuit treatment. Another difficulty is the requirement of broad-bandwidth operation from DC to the maximum bit rate used for data transmission. These are the major reasons that transistor performance no longer directly reflects the circuit and module performance.

Our approach to overcoming the performance limit is the synthesis of distributed and lumped-circuit design technology. A typical example is a DC-to-40-GHz, 9-dB distributed baseband amplifier IC using GaAs MESFETs with an f<sub>T</sub> of 40 GHz [5]. Its circuitry is shown in Fig. 3. Key technologies are 1) the distributed configuration where parasitic capacitance of FETs can be effectively

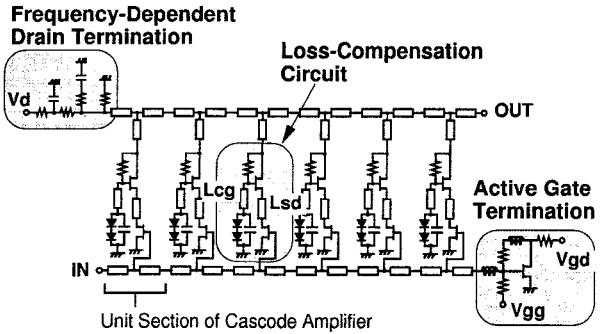


Fig. 3. Distributed baseband amplifier IC.

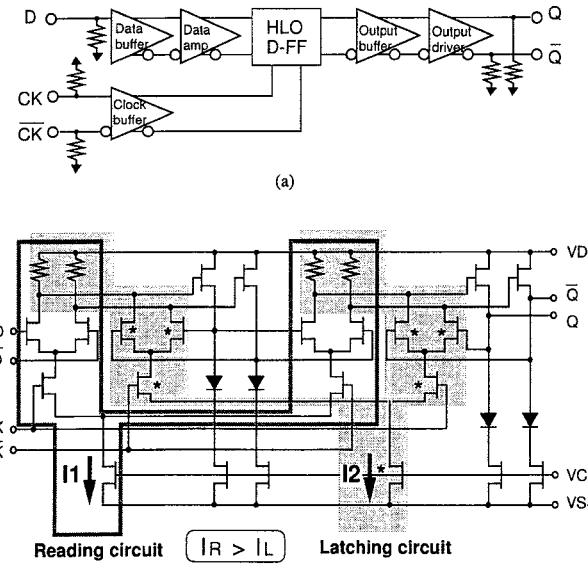


Fig. 4. HLO-DFF type decision circuit: (a) block diagram, (b) HLO-DFF circuit.

incorporated as circuit elements to enable velocity-matched signal transmission, 2) the frequency-dependent biasing termination that can compensate for DC gain degradation caused by the drain conductance of the FETs, 3) the loss compensation circuit where additional transmission lines are utilized to increase its negative resistance that compensate for the loss at high frequencies, and 4) the active gate termination that can improve the noise figure. The record performance of the gain-bandwidth product of 297 GHz is also obtained from other designed chips using InAlAs/InGaAs HEMTs [6]. Packaging these chips is a critical issue. A novel "chip-size cavity" package [7] that minimizes the inner cavity so as to shift up undesirable cavity resonances out the transmission band is one of the solutions.

With regard to digital ICs, a 40-Gb/s Data selector [8] and a D-type FF [9] have been developed using HBT

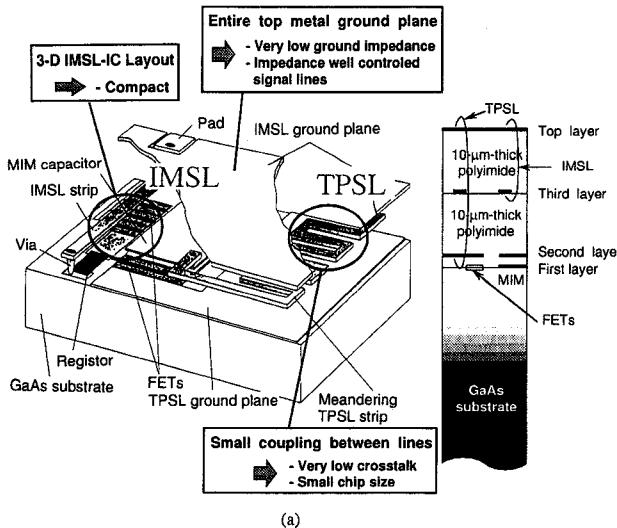


Fig. 5. New multilayer interconnection IC structure: (a) IMSL-IC structure, (b) flip-chip bonding. IML inverted microstrip line, TPSL triplate strip line.

processes and conventional circuit configurations. A 19-Gb/s new HLO-FF decision circuit has also been developed (Fig. 4) by using a commercial 0.2- $\mu$ m gate GaAs MESFET process [10], which is 45% faster than conventional decision circuits with master-slave D-FF. However, these are results of on-wafer measurements. Assuming a sufficient device potential, standard double Au interconnection layers and Au ribbon bonding, decision sensitivity for packaged chips is estimated to exceed 150 mV at 40-Gb/s operation due to undesirable ground impedance and crosstalks. This would not be acceptable.

Our proposal to overcome the parasitic limit is a multilayer interconnection structure with thick polyimide insulators based on face-down bump bonding assembly (Fig. 5). This can provide 1) impedance-well-controllable, parasitic-free inverted microstrip lines, and 2) high isolation due to perfect planer ground formation with the top metal layer and bump grid array. This structure promises stable circuit operation at over 100-GHz. Details will be presented by Yamaguchi at a MTT-S session [11].

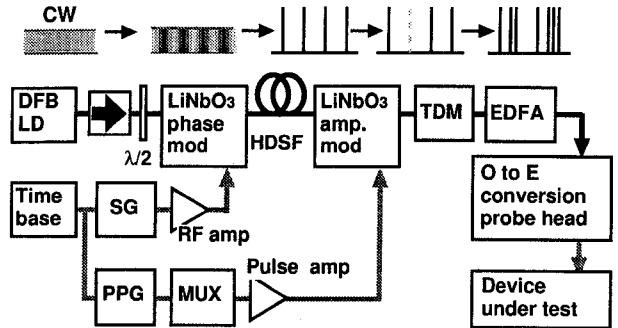


Fig. 6. Optoelectronic pulse-pattern generator. HDSF highly dispersion shifted fiber, SG synthesized signal generator, PPG electronic pulse-pattern generator.

The remaining issues on future high-speed IC design are 1) the designability of structure-dependent parasitic effect, 2) chip-size cavity resonance, and 3) a distributed design approach for digital ICs.

#### IV. MEASUREMENT TECHNOLOGY

To characterize high-speed ICs under actual operating conditions, large-signal pulse pattern response measurement as well as small-signal vector network analysis is essential. Currently available electronic instruments such as pulse pattern generators ( $\leq 15$  Gb/s) and sampling oscilloscopes ( $\leq 50$  GHz), however, cannot meet this requirement. Optoelectronic techniques have therefore been introduced.

We developed a pulse-rate tunable, fully electrically controllable optoelectronic random pulse generator (PPG) [12]. Figure 6 shows the block diagram. RZ pulse trains with a minimum duration of 5 ps are generated from a 1.55- $\mu$ m CW laser light by electrooptic phase modulation and chirping compensation using a dispersion-shifted fiber. A specific pulse pattern train is obtained by modulating the amplitude, and a time-division multiplexer is used to quadruple the bit rate. Pulse rate tunability from 10 to 72 Gb/s has been achieved. The maximum bit rate is now limited by the bandwidth of phase and amplitude modulators and is 18 GHz. The optical signal is introduced to an optical-to-electrical conversion stimulus probe head (Fig. 7). A 110-Hz bandwidth, 0.6-A/W waveguide p-i-n photodiode [13] was used as the O-E conversion device. The measured electrical bandwidth was 50 GHz, which is currently limited by the dispersion along the coplaner waveguide in the probe head.

We configured a prototype of optoelectronic characterization system (Fig. 8). It consists of the OE-PPG, the OE probe, and an electrooptic sampler (EOS) [14]. This was applied to on-wafer characterization for the DC-to-60GHz band HEMT amplifier.

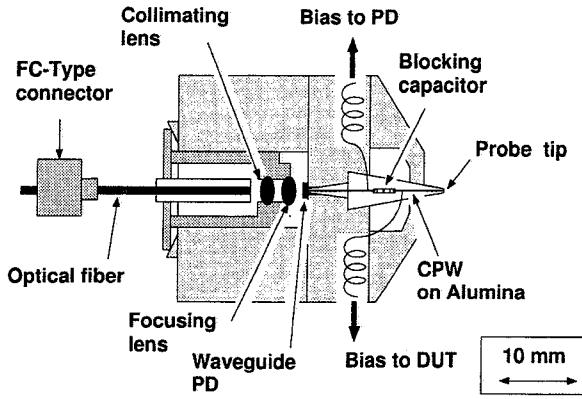


Fig. 7. Optoelectronic conversion active stimulus probe head (bottom view). Inductors are assembled inside the metal block.

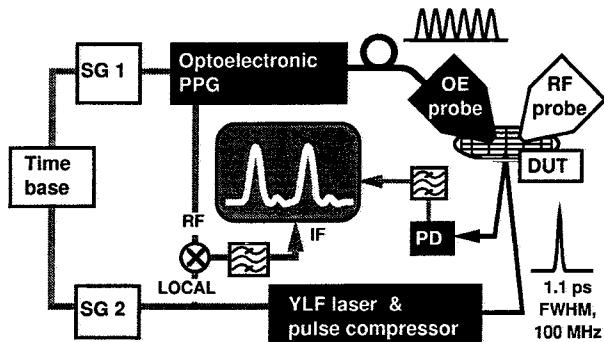


Fig. 8. Optoelectronic IC characterization system.

Figure 9 shows the waveforms measured at the input and output pads when a 64-Gb/s, 120-mVpp repetitive 8-bit pattern "10110100" was injected. Although the input pulse itself is degraded due to undesirable dispersion of the CPW, the 64-Gb/s pulse pattern is successfully observed. The measured waveform revealed very important but never-before observed large-signal characteristics: waveform distortion and gain saturation (1.5 dB smaller than the small-signal measurement results obtained using a network analyzer). If the signal-to-noise ratio of EOS can be improved by orders of magnitude, eye opening and bit error rate measurement will also become feasible.

## V. CONCLUSION

In conclusion, synergistic advancement in electronic and photonic process and in design and measurement technologies will break through the speed barrier and bring 40-Gb/s/channel or more transmission to the real world in a very near future.

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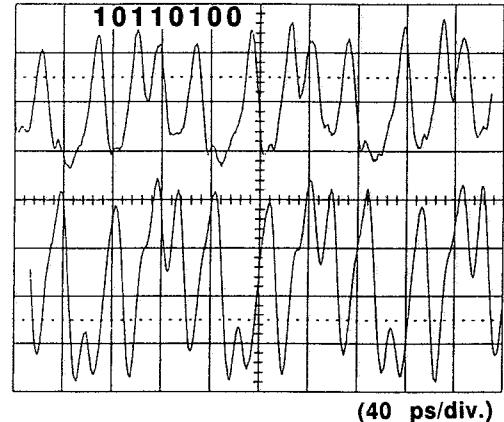


Fig. 9. Typical pulse-pattern response (lower trace: 67.5 mV/div.) of a wideband HEMT amplifier to 64-Gb/s, 120-mVpp input (upper trace: 45 mV/div.). The input pulse has a repetitive 8-bit pattern (10110100).

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